IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for making a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a polysilicon layer on the dielectric layer; and

etching the polysilicon layer to generate a patterned polysilicon layer that has an upper surface, ~~and~~ a lower surface, and at least one sidewall, the upper surface having a first width that is less than or equal to about 45 angstroms, ~~and~~ the lower surface having a second width that is less than or equal to about 40 angstroms, and the sidewall meeting a plane of the dielectric layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall;

wherein the first width is at least about 5 angstroms greater than the second width.

2. (Original) The method of claim 1 further comprising placing the substrate, after it is covered with the dielectric layer and the polysilicon layer, on a chuck that is positioned within a high density plasma etch tool prior to etching the polysilicon layer.

3. (Original) The method of claim 2 wherein the dielectric layer is electrically charged when the polysilicon layer is etched.

4. (Original) The method of claim 3 wherein the dielectric layer comprises a material that is selected from the group consisting of silicon dioxide and a nitrided silicon dioxide and is sufficiently thick to maintain an electric charge for substantially the entire time that the polysilicon layer is etched, the polysilicon layer is between about 100 and about 2,000 angstroms thick, and the polysilicon layer is etched by exposing the polysilicon layer to a plasma derived from chlorine, hydrogen bromide, oxygen, and argon.

5. (Original) The method of claim 4 wherein RF bias power of less than about 100 watts is applied to the chuck as the polysilicon layer is etched.

6. (Original) The method of claim 1 further comprising forming a masking layer on the polysilicon layer prior to etching the polysilicon layer.

7. (Original) The method of claim 6 wherein the masking layer is created at least in part by forming a silicon nitride layer that is between about 100 angstroms and about 500 angstroms thick on the polysilicon layer, then etching the silicon nitride layer by exposing that layer to a plasma.

8. (Original) The method of claim 1 wherein the dielectric layer is a high-k dielectric layer.

9. (Currently Amended) A method for making a semiconductor device comprising:

forming a silicon dioxide layer on a substrate;

forming on the silicon dioxide layer a polysilicon layer that is between about 100 and about 2,000 angstroms thick;

forming a first silicon nitride layer that is between about 100 angstroms and about 500 angstroms thick on the polysilicon layer;

etching the first silicon nitride layer to create a hard mask; and

etching the polysilicon layer to generate a patterned polysilicon layer that has an upper surface, ~~and~~ a lower surface, and at least one sidewall, the upper surface having a first width that is less than or equal to about 45 angstroms, ~~and~~ the lower surface having a second width that is less than or equal to about 40 angstroms, and the sidewall meeting a plane of the silicon dioxide layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall;

wherein the first width is at least about 5 angstroms greater than the second width.

10. (Original) The method of claim 9 further comprising:

etching the silicon dioxide layer after the polysilicon layer is etched to generate a patterned silicon dioxide layer;

depositing a second silicon nitride layer on the substrate, the hard mask, and the patterned polysilicon layer;

removing the second silicon nitride layer from part of the substrate to form first and second spacers on opposite sides of the patterned polysilicon layer;

removing the hard mask, the patterned polysilicon layer, and the patterned silicon dioxide layer to generate a trench that is positioned between the first and second spacers;

forming a high-k gate dielectric layer on the substrate at the bottom of the trench; and

filling at least part of the trench with a metal layer that is formed on the high-k gate dielectric layer.

11. (Original) The method of claim 10 wherein:

the high-k gate dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate; and

the metal layer fills the entire trench and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

12. (Original) The method of claim 9 wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and has a workfunction that is between about 3.9 eV and about 4.2 eV.

13. (Original) The method of claim 9 wherein the metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and has a workfunction that is between about 4.9 eV and about 5.2 eV.

14. (Original) The method of claim 10 further comprising:

forming a dielectric layer on the hard mask and the substrate after forming the first and second spacers;

applying a chemical mechanical polishing process to remove the dielectric layer from the hard mask prior to removing the hard mask, the patterned polysilicon layer, and the patterned silicon dioxide layer to generate the trench;

filling only part of the trench with a workfunction metal that is between about 50 and about 1,000 angstroms thick; and

forming on the workfunction metal a trench fill metal that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride.

15. (Currently Amended) A method for making a semiconductor device comprising:

forming a nitrided silicon dioxide layer on a substrate;

forming on the nitrided silicon dioxide layer a polysilicon layer that is between about 100 and about 2,000 angstroms thick;

forming a first silicon nitride layer that is between about 100 and about 500 angstroms thick on the polysilicon layer;

etching the first silicon nitride layer, the polysilicon layer, and the nitrided silicon dioxide layer, to form a hard mask, a patterned polysilicon layer, and a patterned nitrided silicon dioxide layer, wherein a sidewall of the patterned polysilicon layer meets a plane of the patterned nitrided silicon dioxide layer at an angle that is less than about 87 degrees but sufficiently wide to enable a spacer to be formed on the sidewall;

depositing a second silicon nitride layer on the substrate, the hard mask and on opposite sides of the patterned polysilicon layer;

removing the second silicon nitride layer from part of the substrate and from the hard mask to form first and second spacers on opposite sides of the patterned polysilicon layer;

forming a dielectric layer on the hard mask and on the substrate;

removing the dielectric layer from the hard mask;

removing the hard mask, the patterned polysilicon layer and the patterned nitrided silicon dioxide layer to generate a trench that is positioned between the first and second spacers;

forming a high-k gate dielectric layer on the substrate at the bottom of the trench; and

filling at least part of the trench with a metal layer that is formed on the high-k gate dielectric layer;

wherein the nitrided silicon dioxide layer maintains an electric charge for substantially the entire time that the polysilicon layer is etched.

16. (Original) The method of claim 15 wherein the patterned polysilicon layer has an upper surface and a lower surface, the upper surface having a first width that is less than or equal to about 45 angstroms, the lower surface having a second width that is less than or equal to about 40 angstroms, and the first width being at least about 5 angstroms greater than the second width.

17. (Original) The method of claim 15 wherein:

the high-k gate dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate; and

the metal layer fills the entire trench and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum,

aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

18. (Original) The method of claim 15 wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and has a workfunction that is between about 3.9 eV and about 4.2 eV.

19. (Original) The method of claim 15 wherein the metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and has a workfunction that is between about 4.9 eV and about 5.2 eV.

20. (Original) The method of claim 15 wherein:

a chemical mechanical polishing process is used to remove the dielectric layer from the hard mask; and

the metal layer serves as a workfunction metal that fills only part of the trench and is between about 50 and about 1,000 angstroms thick; and

further comprising forming on the metal layer a trench fill metal that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride.